REMARKS/ARGUMENTS

Claims 1-21 are pending and rejected in this application. Claims 1, 3-8, 13-14, 17 and 19-20 have been amended.

Claims 1, 14, 16, 17, 19, and 20 are rejected under 35 U.S.C. §102(b) as being anticipated by Hammerstrom, US Patent 5,369,773. Claims 2 and 9-12 are rejected under 35 U.S.C. §103(a) as being unpatentable over Hammerstrom, US Patent 5,369,773. Claims 3-8, 13, 15, 18, and 21 are rejected under 35 U.S.C. §103(a) as being unpatentable over Hammerstrom, US Patent 5,369,773, in view of Rotenburg et al., Trace Cache: A Low Latency Approach to High Bandwidth Instruction Fetching.

Claim Rejections Under 35 U.S.C. §102(b)

The Hammerstrom patent, cited by Examiner, teaches a neural network using virtual zeros. The patent generally describes a means for conserving memory by not filling the memory addresses of a sparse matrix with superfluous zeroes. When the disclosure of Hammerstrom is compared with Applicant's claimed invention, it is apparent that it is describing a significantly different technology.

Applicant's claimed invention includes "a Register Alias Table (RAT) to store an instruction register map." Examiner asserts that Hammerstrom teaches this element in the following portion of its disclosure:

> If a non-zero-value data block, as depicted in FIG. 4, having any non-zero bit 50, is input over input bus 44, the non-zero values are detected by counter 38 and the entire block is stored in memory unit 40 as conventional data, including zero bits. Address register 34 is operable to "map" memory to provide the location of the non-zero data blocks, as well as to provide "phantom" addresses for zero-value data blocks.

This portion of Hammerstrom does not teach a RAT for storing an instruction register map, but rather, it teaches a method for reading and writing actual data and storing memory addresses of actual data, not instructions.

Figure 6 provides an overview of what is being taught in the Hammerstrom patent. The rotation register contains either a 0 or a 1 depending on whether or not a data string contains a non-zero value. If the rotation register contains a zero, then the data string contains no non-zero values. If, however, it contains a 1, then the data string contains non-zero values, and the entire data string is stored in memory. As is evident from figure 6, only strings containing non-zero values are actually stored in physical memory, thus reducing the amount of memory needed to store a sparse matrix. Examiner asserts that element 34 of the Hammerstrom disclosure teaches a RAT for storing an instruction register map, but element 34, in actuality, is nothing more than a map of addresses in virtual memory that contain the locations of actual non-zero value data in the physical memory. Neither element 34, nor any portion of the Hammerstrom patent, contain a RAT for storing an instruction register map.

Applicant further claims "a Zeroing Instruction Logic (ZIL) unit to detect a zeroing instruction and modify said RAT with a pointer to said physical zero register." Figure 6 makes it clear that the method taught in the Hammerstrom patent does not teach this claim limitation. As argued above, applicant asserts that Hammerstrom does not teach a RAT, but assuming *arguendo* that element 34 could be considered a RAT, Hammerstrom never teaches modifying that RAT with a pointer to a physical zero register. Element 34 contains a map of the locations of non-zero value data strings, not a pointer to a physical zero register. (*See* column 5, lines 12-19).

On page 2 of the Office Action, Examiner paraphrases this claim element as " . . . modifying the subsequent instruction to account for the deleted zeroing instruction." Examiner does not actually state where in Hammerstrom she believes the modifying of the RAT with a pointer to a physical zero register is actually taught. For at least the following reasons, applicant asserts that the Hammerstrom patent does not teach multiple elements of independent claim 1, and the rejection under 35 U.S.C. §102(b) should, therefore, be withdrawn.

Independent claims 14 and 17 contain elements that are either the same as, or highly similar to, those elements of claim 1 that are not taught in Hammerstrom. Applicant respectfully submits, for at least all the same reasons mentioned with regard to claim 1, the 35 U.S.C. §102(b) rejections of independent claims 14 and 17 should similarly be withdrawn. Additionally, applicant submits that dependent claims 3-8, 13, 15-16, and 18-21 are allowable as depending from independent claims 1, 14, and 17.

Claim Rejections Under 35 U.S.C. §103(a)

Claims 2 and 9-12 depend from allowable independent claim 1. Accordingly, Applicant respectfully requests that the Examiner's rejection under 35 U.S.C. §103(a) be withdrawn.

For all the above reasons, the Applicant respectfully submits that this application is in condition for allowance. A Notice of Allowance is earnestly solicited.

The Examiner is invited to contact the undersigned at (408) 975-7500 to discuss any matter concerning this application.

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The Office is hereby authorized to charge any additional fees or credit any overpayments under 37 C.F.R. §1.16 or §1.17 to Deposit Account No. **11-0600**.

Respectfully submitted,

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